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EXAMINER	
THANGAVELU, KANDASAMY	

ART UNIT	PAPER NUMBER
2123	19

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/273,560	HASEGAWA, TAKUMI	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' Amendment mailed on September 4, 2003. Claims 1-4 of the application were amended. Claims 1-4 of the application are pending. This office action is made non-final.

Response to Amendments

2. Applicants' amendments, filed on September 4, 2003 have been considered. Applicant's arguments with respect to claim rejections under 35 USC 103 (a) are not persuasive. New claim rejections have been included in this Office Action under 35 USC 112 First paragraph and 35 USC 112 Second Paragraph.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. §112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-4 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled

in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

This is because claims 1-4 include limitations involving logical state and current logical state, which are not described anywhere in the specification and therefore constitute ***new material***.

Claim 1 states in part, "said delay information for said at least one circuit is based upon input terminal signal transition type and logical state as represented by said logical operation information for said at least one circuit, and

when making a delay analysis of the logic circuit comprising said at least one circuit, a delay time is selected from said delay time information according to input terminal signal transition type and current logical state of said at least one circuit".

The specification describes on Page 5, Lines 2-6, delay time information stored in the library, according to the logical operation of the basic circuit. However, the specification does not describe anywhere the delay information being stored in the library based upon the logical state represented by the logical operation information. The specification also does not describe anywhere how the logical state is derived from the logical operation information and what the logical state is. The specification also does not describe what the current logical state is and how it is different from the logical state as represented by said logical operation information for said at least one circuit.

Claim 2 states in part, "said delay information for said at least one circuit is based upon input terminal signal transition type and logical state as represented by said logical operation information for said at least one circuit, and

when making a delay analysis of the logic circuit, a delay time between an input terminal and an output terminal of said at least one circuit is selected from said delay time information according to input terminal signal transition type and current logical state of said at least one circuit".

The specification describes on Page 5, Lines 2-6, delay time information stored in the library, according to the logical operation of the basic circuit. However, the specification does not describe anywhere the delay information being stored in the library based upon the logical state represented by the logical operation information. The specification also does not describe anywhere how the logical state is derived from the logical operation information and what the logical state is. The specification also does not describe what the current logical state is and how it is different from the logical state as represented by said logical operation information for said at least one circuit.

Claim 3 states in part, "said delay information for said at least one circuit is based upon input terminal signal transition type and a logical state as represented by said logical operation information for said at least one circuit, and

if the logic circuit comprises said at least one circuit, selecting the delay time of said at least one circuit from said delay time information according to input terminal signal transition type and current logical state of said at least one circuit".

The specification describes on Page 5, Lines 2-6, delay time information stored in the library, according to the logical operation of the basic circuit. However, the specification does not describe anywhere the delay information being stored in the library based upon the logical state represented by the logical operation information. The specification also does not describe anywhere how the logical state is derived from the logical operation information and what the logical state is. The specification also does not describe what the current logical state is and how it is different from the logical state as represented by said logical operation information for said at least one circuit.

Claim 4 states in part, "said delay information for said at least one circuit is based upon input terminal signal transition type and a logical state as represented by said logical operation information for said at least one circuit, and

if the logic circuit comprises said at least one circuit, selecting the delay time of said at least one circuit from said delay time information according to input terminal signal transition type and current logical state of said at least one circuit".

The specification describes on Page 5, Lines 2-6, delay time information stored in the library, according to the logical operation of the basic circuit. However, the specification does not describe anywhere the delay information being stored in the library based upon the logical state represented by the logical operation information. The specification also does not describe anywhere how the logical state is derived from the logical operation information and what the logical state is. The specification also does not describe what the current logical state is and how

it is different from the logical state as represented by said logical operation information for said at least one circuit.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 states in part, "said delay information for said at least one circuit is based upon input terminal signal transition type and logical state as represented by said logical operation information for said at least one circuit, and

when making a delay analysis of the logic circuit comprising said at least one circuit, a delay time is selected from said delay time information according to input terminal signal transition type and current logical state of said at least one circuit".

In this claim the system means for storing in the library said delay information for said at least one circuit based upon logical state as represented by said logical operation information for said at least one circuit is vague and indefinite. The system means for selecting delay time from said delay time information according to current logical state of said at least one circuit is vague and indefinite.

Claim 2 states in part, "said delay information for said at least one circuit is based upon input terminal signal transition type and logical state as represented by said logical operation information for said at least one circuit, and

when making a delay analysis of the logic circuit, a delay time between an input terminal and an output terminal of said at least one circuit is selected from said delay time information according to input terminal signal transition type and current logical state of said at least one circuit".

In this claim the system means for storing in the library said delay information for said at least one circuit based upon logical state as represented by said logical operation information for said at least one circuit is vague and indefinite. The system means for selecting delay time from said delay time information according to current logical state of said at least one circuit is vague and indefinite.

Claim 3 states in part, "said delay information for said at least one circuit is based upon input terminal signal transition type and a logical state as represented by said logical operation information for said at least one circuit, and

if the logic circuit comprises said at least one circuit, selecting the delay time of said at least one circuit from said delay time information according to input terminal signal transition type and current logical state of said at least one circuit".

In this claim the system means for storing in the library said delay information for said at least one circuit based upon logical state as represented by said logical operation information for said at least one circuit is vague and indefinite. The system means for selecting delay time from

said delay time information according to current logical state of said at least one circuit is vague and indefinite.

Claim 4 states in part, "said delay information for said at least one circuit is based upon input terminal signal transition type and a logical state as represented by said logical operation information for said at least one circuit, and

if the logic circuit comprises said at least one circuit, selecting the delay time of said at least one circuit from said delay time information according to input terminal signal transition type and current logical state of said at least one circuit".

In this claim the system means for storing in the library said delay information for said at least one circuit based upon logical state as represented by said logical operation information for said at least one circuit is vague and indefinite. The system means for selecting delay time from said delay time information according to current logical state of said at least one circuit is vague and indefinite.

Claim Interpretations

7. The applicant has modified the claims 1-4 by including new terms logical state and current logical state, which are not described anywhere in the specification. So there is no basis in the specification for the limitations,

"said delay information for said at least one circuit is based upon input terminal signal transition type and a logical state as represented by said logical operation information for said at least one circuit"; and

"if the logic circuit comprises said at least one circuit, selecting the delay time of said at least one circuit from said delay time information according to input terminal signal transition type and current logical state of said at least one circuit".

Accordingly, the Examiner has chosen to give no patentable weight to these two limitations in all claims. Therefore, for the purpose of art rejections, the examiner has interpreted the claims 1-4 as follows:

1. A delay analysis system for making a delay analysis of a logic circuit,

said system having a delay analysis library comprising connection information and delay time information for a plurality of circuits,

wherein for at least one of said plurality of circuits, said library further comprises logical operation information representing correspondence between a logical value of each input terminal of said at least one circuit and a logical value of each output terminal of said at least one circuit, and said delay information for said at least one circuit is based upon input terminal signal transition type; and

when making a delay analysis of the logic circuit comprising said at least one circuit, a delay time is selected from said delay time information according to input terminal signal transition type.

2. A delay analysis system for making a delay analysis of a logic circuit, said system having a delay analysis library comprising connection information and delay time information for a plurality of circuits,

wherein for at least one of said plurality of circuits, said library further comprises logical operation information representing correspondence between a logical value of each input terminal of said at least one circuit and a logical value of each output terminal said at least one circuit, and said delay information for said at least one circuit is based upon input terminal signal transition type; and

when making a delay analysis of a logic circuit, a delay time between an input terminal and an output terminal of said at least one circuit is selected from said delay time information according to input terminal signal transition type.

3. A method for making a delay analysis of a logic circuit, comprising the steps of:

referencing a delay analysis library for a plurality of circuits, said delay analysis library comprising connection information, delay time information and logic operation information representing correspondence between a logical value of each input terminal and a logical value of each output terminal of at least one of said plurality of circuits, said delay information for said at least one circuit is based upon input terminal signal transition type; and

if the logic circuit comprises said at least one circuit, selecting the delay time of said at least one circuit from said delay time information according to input terminal signal transition type.

4. A computer-readable medium having stored thereon a program for executing:

(a) a process step comprising:

referencing a delay analysis library for a plurality of circuits, said delay analysis library comprising connection information, delay time information and logic operation information representing correspondence between a logical value of each input terminal and a logical value of each output terminal of each one of said plurality of circuits, said delay information for said at least one circuit is based upon input terminal signal transition type; and

if the logic circuit comprises said at least one circuit, selecting the delay time of said at least one circuit from said delay time information according to input terminal signal transition type;

(b) a process step of performing a delay calculation using said selected delay time as a propagation delay time of said at least one circuit.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

9. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Blinne et al. (BL)** (U.S. Patent 5,274,568) in view of **Hasegawa (HAS)** (U.S. Patent 6,041,168) and further in view of **Hasegawa (HS)** (U.S. Patent 5,528,511).

10.1 **BL** teaches method of estimating logic cell delay time. Specifically, as per Claim 1, **BL** teaches the delay analysis system for making a delay analysis of a logic circuit (Col 1, Lines 7-13);

the system having a delay analysis library (Col 1, Lines 9-13); and

comprising connection information and delay time information for a plurality of circuits (Col 1, Lines 39-40; Col 1, Lines 60-62; Col 1, Lines 45-48).

BL does not expressly teach that for at least one of the plurality of circuits, the library further comprises logical operation information. **HAS** teaches that for at least one of the plurality of circuits, the library further comprises logical operation information (Col 1, Lines 58-61 and Col 2, Lines 31-35), as delay verification time can be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information (Col 2, Lines 28-35). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** with the system of **HAS** that included for at least one of the plurality of circuits, the library further comprising logical operation information, as delay verification time could be shortened and high

speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information.

BL and **HAS** do not expressly teach the logical operation information representing correspondence between a logical value of each input terminal of the at least one circuit and a logical value of each output terminal of the at least one circuit. **HS** teaches that the logical operation information representing correspondence between a logical value of each input terminal of the at least one circuit and a logical value of each output terminal of the at least one circuit (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** and **HAS** with the system of **HS** that included the logical operation information representing correspondence between a logical value of each input terminal of the at least one circuit and a logical value of each output terminal of the at least one circuit, as this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

BL does not expressly teach that the delay information for the at least one circuit is based upon input terminal signal transition type; and when making a delay analysis of the logic circuit comprising the at least one circuit, a delay time is selected from the delay time information according to input terminal signal transition type. **HS** teaches that the delay information for the at least one circuit is based upon input terminal signal transition type; and when making a delay analysis of the logic circuit comprising the at least one circuit, a delay time is selected from the delay time information according to input terminal signal transition type (Col 2, Lines 30-42; Col

3, Lines 5-26), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** with the system of **HS** that included the delay information for the at least one circuit being based upon input terminal signal transition type; and when making a delay analysis of the logic circuit comprising the at least one circuit, a delay time was selected from the delay time information according to input terminal signal transition type, as this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

10.2 As per Claim 2, **BL** teaches the delay analysis system for making a delay analysis of a logic circuit (Col 1, Lines 7-13);

the system having a delay analysis library (Col 1, Lines 9-13); and

comprising connection information and delay time information for a plurality of circuits (Col 1, Lines 39-40; Col 1, Lines 60-62; Col 1, Lines 45-48).

BL does not expressly teach that for at least one of the plurality of circuits, the library further comprises logical operation information. **HAS** teaches that for at least one of the plurality of circuits, the library further comprises logical operation information (Col 1, Lines 58-61 and Col 2, Lines 31-35), as delay verification time can be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information (Col 2, Lines 28-35). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** with the system of **HAS** that included for at least one of the plurality of circuits, the library further

comprising logical operation information, as delay verification time could be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information.

BL and **HAS** do not expressly teach the logical operation information representing correspondence between a logical value of each input terminal of the at least one circuit and a logical value of each output terminal of the at least one circuit. **HS** teaches that the logical operation information representing correspondence between a logical value of each input terminal of the at least one circuit and a logical value of each output terminal of the at least one circuit (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** and **HAS** with the system of **HS** that included the logical operation information representing correspondence between a logical value of each input terminal of the at least one circuit and a logical value of each output terminal of the at least one circuit, as this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

BL does not expressly teach that the delay information for the at least one circuit is based upon input terminal signal transition type; and when making a delay analysis of a logic circuit, a delay time between an input terminal and an output terminal of the at least one circuit is selected from the delay time information according to input terminal signal transition type. **HS** teaches that the delay information for the at least one circuit is based upon input terminal signal transition type; and when making a delay analysis of a logic circuit, a delay time between an

input terminal and an output terminal of the at least one circuit is selected from the delay time information according to input terminal signal transition type (Col 2, Lines 30-42; Col 3, Lines 5-26), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **BL** with the system of **HS** that included the delay information for the at least one circuit being based upon input terminal signal transition type; and when making a delay analysis of a logic circuit, a delay time between an input terminal and an output terminal of the at least one circuit was selected from the delay time information according to input terminal signal transition type, as this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

10.3 As per Claim 3, **BL** teaches a method for making a delay analysis of a logic circuit (Col 1, Lines 7-13); comprising the steps of:

referencing a delay analysis library for a plurality of circuits (Col 1, Lines 9-13);

the delay analysis library comprising connection information, delay time information (Col 1, Lines 39-40; Col 1, Lines 60-62; Col 1, Lines 45-48).

BL does not expressly teach the delay analysis library comprising logic operation information representing correspondence between a logical value of each input terminal and a logical value of each output terminal of at least one of the plurality of circuits. **HAS** teaches library comprising logic operation information (Col 1, Lines 58-61 and Col 2, Lines 31-35), as delay verification time can be shortened and high speed delay verification achieved by

calculating delay time based on logic information, connecting information and delay information (Col 2, Lines 28-35). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **BL** with the method of **HAS** that included the library comprising logic operation information, as delay verification time could be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information.

BL and **HAS** do not expressly teach logic operation information representing correspondence between a logical value of each input terminal and a logical value of each output terminal of at least one of the plurality of circuits. **HS** teaches logic operation information representing correspondence between a logical value of each input terminal and a logical value of each output terminal of at least one of the plurality of circuits (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **BL** and **HAS** with the method of **HS** that included logic operation information representing correspondence between a logical value of each input terminal and a logical value of each output terminal of at least one of the plurality of circuits, as this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

BL does not expressly teach the delay information for the at least one circuit is based upon input terminal signal transition type; and if the logic circuit comprises the at least one circuit, selecting the delay time of the at least one circuit from the delay time information

according to input terminal signal transition type. **HS** teaches the delay information for the at least one circuit is based upon input terminal signal transition type; and if the logic circuit comprises the at least one circuit, selecting the delay time of the at least one circuit from the delay time information according to input terminal signal transition type (Col 2, Lines 30-42; Col 3, Lines 5-26), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the method of **BL** with the method of **HS** that included the delay information for the at least one circuit being based upon input terminal signal transition type; and if the logic circuit comprises the at least one circuit, selecting the delay time of the at least one circuit from the delay time information according to input terminal signal transition type, as this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

10.4 As per Claim 4, **BL** teaches a computer-readable medium having stored thereon a program for executing a process step (Col 2, Lines 42-50); comprising:

referencing a delay analysis library for a plurality of circuits (Col 1, Lines 9-13);

the delay analysis library comprising connection information, delay time information (Col 1, Lines 39-40; Col 1, Lines 60-62; Col 1, Lines 45-48).

BL does not expressly teach the delay analysis library comprising logic operation information representing correspondence between a logical value of each input terminal and a logical value of each output terminal of each one of the plurality of circuits. **HAS** teaches that the library comprising logical operation information (Col 1, Lines 58-61 and Col 2, Lines 31-35),

as delay verification time can be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information (Col 2, Lines 28-35). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer-readable medium of **BL** with the computer-readable medium of **HAS** that included the library comprising logical operation information, as delay verification time could be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information.

BL and **HAS** do not expressly teach the logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of the plurality of circuits. **HS** teaches that the logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of the plurality of circuits (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer-readable medium of **BL** and **HAS** with the computer-readable medium of **HS** that included the logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of the plurality of circuits, as this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

BL does not expressly teach the delay information for the at least one circuit is based upon input terminal signal transition type; and if the logic circuit comprises the at least one circuit, selecting the delay time of the at least one circuit from the delay time information according to input terminal signal transition type. **HS** teaches the delay information for the at least one circuit is based upon input terminal signal transition type; and if the logic circuit comprises the at least one circuit, selecting the delay time of the at least one circuit from the delay time information according to input terminal signal transition type (Col 2, Lines 30-42; Col 3, Lines 5-26), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer-readable medium of **BL** with the computer-readable medium of **HS** that included the delay information for the at least one circuit being based upon input terminal signal transition type; and if the logic circuit comprises the at least one circuit, selecting the delay time of the at least one circuit from the delay time information according to input terminal signal transition type, as this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

BL does not expressly teach a computer-readable medium having stored thereon a program for executing a process step of performing a delay calculation using selected delay time as a propagation delay time of at least one circuit. **HS** teaches a computer-readable medium having stored thereon a program for executing a process step of performing a delay calculation using selected delay time as a propagation delay time of at least one circuit (Col 3, Lines 5-26), as this provides correct delay time even when either of rise or fall of the signal has no effect in a

delay time computation process (Col 2, Lines 61-65). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the computer-readable medium having stored thereon a program of **BL** with the computer-readable medium having stored thereon a program of **HS** that included executing a process step of performing a delay calculation using selected delay time as a propagation delay time of at least one circuit, as this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process.

Arguments

11.1 As per the applicants' argument that "the combination of Blinne et al., Hasegawa '168 and Hasegawa '511 fails to teach or suggest a delay analysis library comprising delay information for a circuit that is based upon the type of signal transitions present at the circuit's input terminals and the logical state of the circuit as represented by stored logical operation information; the combination of Blinne et al., Hasegawa '168 and Hasegawa '511 does not use input signal transition and logical state information in the same manner as the present invention; in the present invention, delay times are based upon the current logical state of a logic circuit, and type of input signal transitions that are present on the inputs of the logic circuit; a rising edge signal might have two different propagation delay times, based on the logical state of the circuit and the logical states of the input signals", the examiner requests the applicant's attention to the fact that the specification describes on Page 5, Lines 2-6, delay time information stored in the library, according to the logical operation of the basic circuit; however, the specification does not describe anywhere the delay information being stored in the library based upon the logical state

represented by the logical operation information; the specification does not describe anywhere how the logical state is derived from the logical operation information and what the logical state is; the specification does not describe what the current logical state is and how it is different from the logical state as represented by said logical operation information for said at least one circuit.

11.2 As per the applicants' argument that "Blinne et al. do not teach or suggest determining delay time based on the current logical state of a circuit and how input signal transitions will affect that logical state", the examiner requests the applicant's attention to the fact that the specification does not describe anywhere the delay information being computed based upon the current logical state of a circuit; and the specification does not describe anywhere how the current logical state is derived and what the current logical state is.

11.3 As per the applicants' argument that "Hasegawa does not teach or suggest determining delay time based on the current logical state of a circuit and how input signal transitions will affect that logical state", the examiner requests the applicant's attention to the fact that the specification does not describe anywhere the delay information being computed based upon the current logical state of a circuit; and the specification does not describe anywhere how the current logical state is derived and what the current logical state is.

11.4 As per the applicants' argument that "Since Blinne et al., Hasegawa '168 and Hasegawa '511 do not disclose a delay analysis library comprising delay information for a circuit that is based upon the type of signal transitions present at the circuit's input terminals and the logical

state of the circuit as represented by stored logical operation information, Applicants believe that one of skill in the art would not be motivated to combine the three references", the examiner requests the applicant's attention to the fact that the specification describes on Page 5, Lines 2-6, delay time information stored in the library, according to the logical operation of the basic circuit; however, the specification does not describe anywhere the delay information being stored in the library based upon the logical state represented by the logical operation information; and the specification does not describe anywhere how the logical state is derived from the logical operation information and what the logical state is.

11.5 As per the applicants' argument that "none of the references disclose providing delay information for a circuit that is based upon the type of signal transitions present at the circuit's input terminals and the logical state of the circuit as represented by stored logical operation information", the examiner requests the applicant's attention to the fact that the specification describes on Page 5, Lines 2-6, delay time information stored in the library, according to the logical operation of the basic circuit; however, the specification does not describe anywhere the delay information being stored in the library based upon the logical state represented by the logical operation information; and the specification does not describe anywhere how the logical state is derived from the logical operation information and what the logical state is.

11.6 As per the applicants' argument that "none of the references teach or suggest that a delay time is selected from delay time information according to input signal transition type and current logical state of a circuit", the examiner requests the applicant's attention to the fact that the

specification does not describe anywhere the delay information being computed based upon the current logical state of a circuit; and the specification does not describe anywhere how the current logical state is derived and what the current logical state is.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 703-305-0043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
November 15, 2003

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER